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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,970	07/08/2003	Mitchell Alsup	5500-81600	8802

53806 7590 07/01/2009

MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL (AMD)
P.O. BOX 398
AUSTIN, TX 78767-0398

EXAMINER	
GEIB, BENJAMIN P	

ART UNIT	PAPER NUMBER
2181	

NOTIFICATION DATE	DELIVERY MODE
07/01/2009	ELECTRONIC

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MITCHELL ALSUP and GREGORY W. SMAUS

Appeal 2008-001210
Application 10/614,970[1]
Technology Center 2100

Decided: June 30, 2009[2]

Before JAMES D. THOMAS, JOSEPH L. DIXON, and
CAROLYN D. THOMAS, *Administrative Patent Judges.*

C. THOMAS, *Administrative Patent Judge.*

DECISION ON APPEAL

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[1] Application filed July 8, 2003. The real party in interest is Advanced Micro Devices, Inc.

[2] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 CFR § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

I. STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from a final rejection of claims 1-41 mailed July 14, 2006, which are all the claims remaining in the application. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

A. INVENTION

Appellants invented a system and method for implementing a set of microcode operations corresponding to a microcode instruction as a microcode subroutine. A microprocessor includes a dispatch unit configured to dispatch operations and a scheduler coupled to the dispatch unit and configured to schedule dispatched operations for execution. In response to receiving a microcode instruction, the dispatch unit is configured to dispatch a microcode subroutine call operation that specifies a tag identifying a microcode subroutine. (Spec. 61, Abstract.)

B. ILLUSTRATIVE CLAIMS

The appeal contains claims 1-141. Claims 1, 17, 29, 40 and 41 are independent claims. Claims 1 and 29 are illustrative:

> 1. A microprocessor, comprising:
>
> a dispatch unit configured to dispatch operations;
>
> a scheduler coupled to the dispatch unit and configured to schedule dispatched operations for execution;
>
> wherein in response to receiving a microcode instruction, the dispatch unit is configured to dispatch to the scheduler a microcode subroutine call operation that includes a tag identifying a microcode subroutine associated with the microcoded instruction.

29. A method, comprising:

receiving a stream of instructions;

detecting a microcoded instruction within the stream of instructions, wherein the microcoded instruction immediately precedes an other instruction in program order;

in response to said detecting, dispatching a microcode subroutine call operation that identifies a microcode subroutine associated with the microcoded instruction, wherein the microcode subroutine call operation pushes an address of the other instruction onto a stack; and

executing a plurality of operations included in the microcode subroutine, wherein the plurality of operations include a return operation, and wherein execution of the return operation pops the address from the stack.

C. REFERENCES

The references relied upon by the Examiner as evidence in rejecting the claims on appeal are as follows:

Carbine	US 5,630,083	May 13, 1997
Tran	US 5,864,689	Jan. 26, 1999
Harris	US 6,260,138 B1	Jul. 10, 2001
Kling	US 2004/0049657 A1	Mar. 11, 2004 (Filed Sep. 10, 2002)

Rotenberg, et al., *Trace Cache: a Low Latency Approach to High Bandwidth Instruction Fetching*, IEEE 24, 24-34 (1996) (hereinafter "Rotenberg").

Intel Architecture Software Developer's manual, Volume 1: Basic Architecture, Sec. 4.3 (1999) (hereinafter "Intel").

D. REJECTIONS

The Examiner entered the following six (6) rejections which are before us for review:

(1) Claims 1, 15-17, 27-29, 39, and 41 are rejected under 35 U.S.C. § 102(b) as being anticipated by Tran (also referencing "Intel");

(2) Claim 40 is rejected under 35 U.S.C. § 102(b) as being anticipated by Carbine;

(3) Claims 2-6, 18-22, and 30-34 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tran in view of Carbine;

(4) Claims 7, 8, 23, 24, 35, and 36 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tran in view of Carbine and further in view of Rotenberg;

(5) Claims 9, 10, 25, and 37 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tran in view of Kling; and

(6) Claims 11-14, 26, and 38 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tran in view Kling further in view of Harris.

II. FINDINGS OF FACT

The following findings of fact (FF) are supported by a preponderance of the evidence.

Appellants' Specification

1. Appellants disclose that "[o]ften, long running or complex instructions are classified as microcoded instructions. Microcoded instructions are handled by a microcode instruction unit within the microprocessor, which decodes the complex microcoded instruction and

produces a series of less-complex operations for execution by the microprocessor." (Spec., 2, ¶ [0005].)

Tran

2. Tran discloses that the "instruction decode unit 36 stalls upon detection of an instruction to be performed by microcode unit 45, and begins fetching and dispatching instructions again one microcode unit 45 indicates that the routine corresponding to that instruction has completed dispatch." (Col. 4, ll. 36-41.)

3. Tran discloses that "[a] 'subroutine call instruction' is a branch instruction which stores the address of the following instruction within a predefined storage location." (Col. 4, ll. 44-46.)

Carbine

4. Carbine discloses that "[t]he micro-alias registers 562 are particularly useful in long instruction flows, which allows the microcode programmer flexibility in retaining information" (col. 12, ll. 36-38).

5. Carbine discloses that "a common generic microcode routine can be utilized by any of a number of other microcode programs." (col. 12, ll. 51-52.)

6. Carbine discloses that "the MS unit 534 supplies a LOADUAR ('Load Micro-Alias Register') signal that loads the micro-alias register 562, and UARUIP ("Micro-Alias Register Micro-Instruction Pointer") signal that includes two bits to select one of the four Cuops from which to store information." (Col. 12, ll. 24-30.)

7. Carbine discloses that "the programmer has great flexibility to access any register indirectly by accessing the register address within the micro-alias register 562." (Col. 12, ll. 53-56.)

Kling

8. Kling discloses "a processor having a trace cache-based microarchitecture" (page 4, ¶[0032]).

9. In Kling, "information relating to that instruction and the extended register space to which it requires access can be stored in the microcode trace to enable more efficient processing of that instruction" (page 4, ¶[0032]).

Harris

10. Harris discloses that "a pre-decode unit is operable to determine instruction path priorities and to associate a priority tag with each instruction in an instruction cache." (Col. 3, ll. 27-30.)

III. PRINCIPLES OF LAW

In rejecting claims under 35 U.S.C. § 102, "[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation." *Perricone v. Medicis Pharmaceutical Corp.*, 432 F.3d 1368, 1375 (Fed. Cir. 2005), citing *Minn. Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 1565 (Fed. Cir. 1992).

"Anticipation of a patent claim requires a finding that the claim at issue 'reads on' a prior art reference." *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed Cir. 1999) ("In other words, if granting patent

protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art.") *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed Cir. 1999) (internal citations omitted).

"What matters is the objective reach of the claim. If the claim extends to what is obvious, it is invalid under § 103." *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 419 (2007). To be nonobvious, an improvement must be "more than the predictable use of prior art elements according to their established functions." *Id.* at 417.

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness." (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998))). Therefore, we look to Appellants' Brief to show error in the proffered prima facie case. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the Brief has not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

IV. ANALYSIS

Grouping of Claims

In the Brief:

Group I: Appellants essentially argue claims 1, 15-17, 27 and 28 as a group (App. Br. 11-13). For claims 15-17, 27 and 28, Appellants repeat the same argument made for claim 1. We will, therefore, treat claims 15-17, 27 and 28 as standing or falling with claim 1.

Group II: Appellants essentially argue claims 29, 39, and 41 as a group (App. Br. 14-17). For claims 39 and 41, Appellants repeat the same argument made for claim 29. We will, therefore, treat claims 39 and 41 as standing or falling with claim 29.

Group III: Appellants separately argue claim 40 (App. Br. 17-19).

Group IV: Appellants argue claims 2, 18, and 30 as a group (App. Br. 19-21). For claims 18 and 30, Appellants repeat the same argument made for claim 2. We will, therefore, treat claims 18 and 30 as standing or falling with claim 2.

Group V: Appellants essentially argue claims 3, 8, 19, 24, 31 and 36 as a group (App. Br. 21-22: 28). For claims 8, 19, 24, 31 and 36, Appellants repeat the same argument made for claim 3. We will, therefore, treat claims 19 and 31 as standing or falling with claim 3.

Group VI: Appellants argue claims 4, 5, 20, 21, 33, and 34 as a group (App. Br. 22-25). For claims 5, 20, 21, 33, and 34, Appellants repeat the same argument made for claim 4. We will, therefore, treat claims 5, 20, 21, 33, and 34 as standing or falling with claim 4.

Group VII: Appellants argue claims 6, 22, and 32 as a group (App. Br. 25-26). For claims 22 and 32, Appellants repeat the same argument made for claim 6. We will, therefore, treat claims 22 and 32 as standing or falling with claim 6.

Group VIII: Appellants argue claims 7, 23, 35 as a group (App. Br. 26-27). For claims 23 and 35, Appellants repeat the same argument made for claim 7. We will, therefore, treat claims 23 and 35 as standing or falling with claim 7.

Group IX: Appellants argue claims 9, 10, 25, and 37 as a group (App. Br. 28-29). For claims 10, 25, and 37, Appellants repeat the same argument made for claim 9. We will, therefore, treat claims 10, 25, and 37 as standing or falling with claim 9.

Group X: Appellants argue claims 11, 12, 13, 14, 26, and 38 as a group (App. Br. 29-31). For claims 12, 13, 14, 26, and 38, Appellants repeat the same argument made for claim 11. We will, therefore, treat claims 12, 13, 14, 26, and 38 as standing or falling with claim 11.

37 C.F.R. § 41.37(c)(1)(vii). *See also In re Young,* 927 F.2d 588, 590 (Fed. Cir. 1991).

The Anticipation Rejection

We first consider the Examiner's rejection of the claims under 35 U.S.C. § 102(b).

Group I
Claims 1, 15-17, 27, and 28

Appellants contend:

> In Tran, the instruction that is detected is a source-code instruction, e.g., "CALL", having a target address in a particular range. Therefore, Tran does not describe detecting a microcoded instruction, but detecting a non-micro-coded instruction (e.g., a "CALL" instruction) that is used to invoke a subroutine call in order to emulate a microcoded instruction

> (e.g., to emulate an instruction that is not included in the instruction set.)

(App. Br. 11-12.)

Appellants further contend that in the claimed invention, "[i]n response to receiving one (the microcoded instruction), the other (the microcoded subroutine call operation) is dispatched. By contrast, in Tran, the x86 CALL instruction, a source code instruction of the x86 instruction set architecture, is received and is itself dispatched for execution." (App. Br. 13.)

The Examiner found that in Tran "an x86 CALL instruction is a microcoded instruction in that it is performed (at least in part) by the microcode unit. Therefore, Tran has taught receiving/detecting a microcoded instruction (i.e., a CALL instruction)." (Ans. 15-16.)

The Examiner further found that "[a]s noted in appellant's specification, reservation stations are schedulers. Therefore, it follows that Tran has taught that instructions fetched from the instruction cache 32 are decoded by the decode unit 36 and dispatched to reservation stations (i.e., schedulers) within either execute unit 38 or load/store unit 40." (Ans. 16.)

Issue: Have Appellants shown that the Examiner erred in finding that Tran discloses that *"in response to receiving a microcoded instruction, the dispatch unit is configured to dispatch to the scheduler a microcode subroutine call operation,"* as set forth in claim 1?

Appellants' initial contention is that Tran fails to disclose receiving/detecting a microcoded instruction in that Tran's x86 CALL instruction is not a microcoded instruction (App. Br. 11). We disagree.

Our analysis begins with construing the claimed "microcoded instruction" and we shall give this term its broadest reasonable construction in light of the specification as it would be interpreted by one of ordinary skill in the art. *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004). Appellants' Specification simply discloses that microcoded instructions are handled by a microcode unit and are often long running complex instructions (FF 1). Thus, we find that the claimed "microcoded instructions" reasonably includes any complex instruction that can be handled by a microcode unit.

The Examiner found that Tran discloses an x86 CALL instruction that is performed (at least in part) by a microcode unit (Ans. 15-16)(FF 2). Therefore, the Examiner concluded that Tran's x86 CALL instruction reads on a "microcoded instruction." We agree.

Secondly, Appellants contend that Tran fails to disclose "in response to receiving a microcoded instruction, the dispatch unit is configured to dispatch to the scheduler a microcode subroutine call operation." (App. Br. 13.) We disagree.

The Examiner found that the flow of instructions through Trans' processor includes the conveyance of a microcoded subroutine call operation to a reservation station (i.e., a scheduler) (Ans. 16-17.) We find that the claimed *"dispatch to the scheduler a microcoded subroutine call operation"* reads on Trans' instruction flow to the reservation station. Thus, we endorse and adopt the Examiner's findings in the Answer regarding the dispatch limitation.

Thus, Appellants have *not* persuaded us of error in the Examiner's conclusion of anticipation for representative claim 1. Therefore, we affirm

the Examiner's § 102 rejection of independent claim 1 and of claims 15-17, 27, and 28, which fall therewith.

Group II
Claims 29, 39, and 41

Appellants contend that "[n]othing in Tran discloses the microcode subroutine pushing and popping operations on a stack." (App. Br. 16.)

The Examiner found that Tran discloses that the "microcode subroutine executed as part of an x86 CALL instruction concludes with the execution of a subroutine return instruction . . . an x86 RET instruction involves popping the instruction pointer . . . from the stack" (Ans. 19).

Issue: Have Appellants shown that the Examiner erred in finding that Tran discloses that *"the microcode subroutine call operation pushes an address of the other instruction onto a stack,"* as set forth in claim 29?

We endorse and adopt the Examiner's findings that Tran discloses a second format of the x86 CALL instruction that acts as a microcode subroutine call operation that saves the address of the current instruction pointer which involves pushing the address onto a stack (Ans. 19). Specifically, Tran discloses that the call instruction stores the address of the next instruction (i.e., other instruction) in a storage location (FF 3). Thus, the claimed "microcode subroutine call operation pushes an address of the other instruction onto a stack" reads on Trans' storage of the next to be performed instruction into a predefined storage location.

Thus, Appellants have *not* persuaded us of error in the Examiner's conclusion of anticipation for representative claim 29. Therefore, we affirm

the Examiner's § 102 rejection of independent claim 29 and of claims 39 and 41, which fall therewith.

Group III
Claim 40

Appellants contend that "there is nothing in this citation or elsewhere in Carbine that teaches multiple alias table elements or multiple micro-alias registers. Instead, Carbine describes a single micro-alias register (having multiple fields, but not multiple entries), which is loaded with different data dependent on which of four CUOPs is selected by multiplexer 560." (App. Br. 18.) Appellants further contend that "even if multiple generic routines may exist in the system of Carbine, there is nothing in Carbine that teaches dispatching two such routines." (App. Br. 19.)

The Examiner found that "column 12, line 36, of Carbine, which recites 'the micro-alias registers 562 are particularly useful . . .'. Therefore, Carbine clearly has taught multiple micro-alias registers, not just a single micro-alias register as asserted by appellant." (Ans. 20.) The Examiner further found that "Carbine indicates that there are other generic microcode subroutines executed/dispatched." (*Id.*).

Issue: Have Appellants shown that the Examiner erred in finding that Carbine discloses "a first alias table element" and "a second alias table element," as set forth in claim 40?

The Examiner found that Carbine discloses micro-alias registers, in the plural (FF 4). We also find that Carbine's Fig. 5 illustrates at least two micro-alias registers boxes, e.g., element 562 and element 580. Thus, we

find that Carbine discloses at least first and second alias table elements being represented as registers.

The Examiner further found that Carbine discloses a plurality of generic microcode subroutines being used in the system (Ans. 20). Thus, the Examiner concluded that Carbine must dispatch more than one routine. We agree. There is nothing in claim 40 that requires dispatching the operations simultaneously, only that two operations be dispatched. Thus, the claimed dispatching operations in a first/second microcode subroutine reads on Carbine's plurality of generic microcode subroutines that are executed (FF 5).

Thus, Appellants have *not* persuaded us of error in the Examiner's conclusion of anticipation for representative claim 40. Therefore, we affirm the Examiner's § 102 rejection of independent claim 40.

The Obviousness Rejection

We now consider the Examiner's rejection of the claims under 35 U.S.C. § 103(a).

Group IV
Claims 2, 18, and 30

Appellants contend that in Carbine "the LOADUAR ('Load Micro-Alias Register') signal is not an operation dispatched by a dispatch unit to a scheduler (i.e., an operation dispatched for execution). Instead, it is a signal supplied by the microcode sequencing unit 534 to load the micro-alias register from one of four Cuops (as selected by a UARUIP signal)." (App. Br. 20.)

The Examiner found that "the LOADUAR signal loads a micro alias register that holds an address of a register that is to be used as a replacement within a microcode subroutine." (Ans. 21.)

Issue: Have Appellants shown that the Examiner erred in finding that Tran/Carbine discloses dispatching an operation that provides one or more register names?

Carbine discloses supplying (i.e., dispatching) a signal that loads an address into the micro-alias register (FF 6-7). The Examiner found that the claimed "register name" reads on Carbine's address information stored in the micro-alias register. We agree. Thus, Carbine reasonably discloses dispatching an operation that provides register names.

Therefore, Appellants have *not* persuaded us of error in the Examiner's conclusion of obviousness for representative claim 2. Therefore, we affirm the Examiner's § 103 rejection of dependent claim 2, and of claims 18 and 30, which fall therewith.

Group V
Claims 3, 8, 19, 24, 31, and 36

Appellants contend that "there is nothing in Carbine that teaches or suggests that a dispatch unit (i.e., one that performs the functions recited in Appellants' claims) allocates a micro-alias register for any reason. Instead, the micro-alias register is always available to be loaded with information from one of four Cuop registers 550." (App. Br. 22.)

The Examiner found that "[t]he dispatch unit sends a LOADUAR signal to load a micro-alia register, thereby allocating a micro-alias register." (Ans. 22.)

Issue: Have Appellants shown that the Examiner erred in finding that Tran/Carbine discloses allocating an alias table element to store the one or more register names?

Initially, we note that Appellants' arguments and the Examiner's findings suggest that the claimed "alias table element" reads on Carbine's micro-alias register. We also adopt this finding. However, the issue now turns on whether such micro-alias register is allocated to store register names. Carbine discloses that a signal is supplied from the MS unit that allows the micro-alias register to be loaded (FF 6). The Examiner concludes that such "a signal" in essence allocates the register (Ans. 22). We agree. Appellants have not shown how supplying such a "signal" which dictates a load operation/register is distinguishable from allocating a table element.

Therefore, Appellants have *not* persuaded us of error in the Examiner's conclusion of obviousness for representative claim 3. Therefore, we affirm the Examiner's § 103 rejection of dependent claim 3, and of claims 8, 19, 24, 31 and 36, which fall therewith.

Group VI
Claims 4, 5, 20, 21, 33, and 34

Appellants contend that "the Examiner's remarks include the phrase, 'the dispatch unit updates/maintains the micro-alias registers.' Appellants

assert that updating the micro-alias registers is the opposite of maintaining alias table elements." (App. Br. 24.)

The Examiner found that "appellant is reading the term 'maintain' too narrowly. . . . Clearly, updating is a type of maintenance." (Ans. 23.)

Issue: Have Appellants shown that the Examiner erred in finding that the cited art discloses "the dispatch unit is configured to maintain multiple allocated alias table elements at a same time"?

Carbine discloses that the micro-alias registers are used to retain information (FF 4). Thus, under the broadest reasonable interpretation, the claimed "maintain multiple allocated alias table elements" reads on Carbine's ability to retain information in the micro-alias registers.

Therefore, Appellants have *not* persuaded us of error in the Examiner's conclusion of obviousness for representative claim 4. Therefore, we affirm the Examiner's § 103 rejection of dependent claim 4, and of claims 5, 20, 21, 33, and 34, which fall therewith.

Group VII
Claims 6, 22, and 32

Appellants contend that Carbine "teaches away from the limitations of claim 6, in which the one or more register names already stored within a respective alias table element are used to perform replacements in response to detection of a branch misprediction." (App. Br. 26.)

The Examiner found that "[t]he language of claim 6 merely describes the usage of the alias table elements subsequent to a mispredicted branch.

The citation of Carbine given by the Examiner describes this usage of the micro-alias registers subsequent to a mispredicted branch." (Ans. 24.)

Issue: Have Appellants shown that the Examiner erred in finding that Carbine discloses the limitations of claim 6?

We endorse and adopt the Examiner's finding as outlined in the Answer on page 24, as it demonstrates that Carbine discloses the usage of micro-alias register/names subsequent to receiving a branch operation.

Therefore, Appellants have *not* persuaded us of error in the Examiner's conclusion of obviousness for representative claim 6. Therefore, we affirm the Examiner's § 103 rejection of dependent claim 6, and of claims 5, 22 and 32, which fall therewith.

Group VIII
Claims 7, 23, and 35

Appellants contend that "Claim 7 does not recite that a trace cache entry includes 'instructions from the dynamic stream,' but a trace cache entry that includes the microcode subroutine call operation and the one or more register names for use as replacement register names. There is nothing in Rotenburg or the other cited references that teaches a trace entry including these specific elements." (App. Br. 27.)

The Examiner relies upon Rotenburg to teach a trace cache entry that includes instructions from the dynamic instruction stream and "[t]he dynamic instruction stream, as taught by Tran in view of Carbine, includes the microcode subroutine call operation and the one or more register names for use as replacement register names." (Ans. 25.)

Issue: Have Appellants shown that the Examiner erred in finding that the combination of Tran, Carbine, and Rotenburg discloses the disputed features of claim 7?

Again, we endorse and adopt the Examiner's finding on page 25 of the Answer regarding the above disputed features of claim 7. Appellants have not demonstrated that such combined findings are distinguishable from the claimed invention, as all the elements are shown in the cited combination of references.

Therefore, Appellants have *not* persuaded us of error in the Examiner's conclusion of obviousness for representative claim 7. Therefore, we affirm the Examiner's § 103 rejection of dependent claim 7, and of claims 23 and 35, which fall therewith.

Group X
Claims 9, 10, 25, and 37

Appellants contend that Kling "mentions the existence of a 'microcode trace' but does not teach or suggest that a microcode subroutine is stored in one or more such traces." (App. Br. 29.)

The Examiner found that "as indicated by the name 'microcode trace,' the trace comprises microcode instructions. A subroutine is merely a sequence of instructions. Therefore, the microcode inherently includes at least one microcode subroutine." (Ans. 26.)

Issue: Have Appellants shown that the Examiner erred in finding that Kling discloses a microcode subroutine stored as one or more microcode traces?

Kling discloses that instruction information can be stored in the microcode trace (FF 8-9). The Examiner reasons that such stored instruction information can reasonably include a microcode subroutine. Given that Tran discloses subroutines (FF 3) and Tran is combined with Kling, we find that the claimed "microcode subroutine is stored as one or more microcode traces" reads on Tran/Kling's above-noted disclosures.

Therefore, Appellants have *not* persuaded us of error in the Examiner's conclusion of obviousness for representative claim 9. Therefore, we affirm the Examiner's § 103 rejection of dependent claim 9, and of claims 10, 25, and 37, which fall therewith.

Group XI
Claims 11, 12, 13, 14, 26, and 38

Appellants contend "that the priority tag of Harris is not an indication of liveness, as the term would be understood by one of ordinary skill in the art or as used in Appellants' specification." (App. Br. 30.) Appellants further contend that "since Tran does not teach that microcode subroutines are stored in microcode traces, the combination of Tran and Harris cannot teach or suggest additional limitations on such microcode traces." (App. Br. 31.)

The Examiner found that Harris teaches a priority tag that acts as a liveness indication (Ans. 13.) The Examiner also found that Tran and Kling teach that microcode operations are stored in one or more microcode traces (*Id.*).

Issue: Have Appellants shown that the Examiner erred in finding that the combination of cited art discloses a liveness indication and microcoded subroutines stored in microcode traces?

As for the claimed "liveness indication," we note that Appellants' Specification discloses that a "liveness indication" identifies the branch operations within the microcode trace (Spec., ¶ [0010]). Thus, we find that a "liveness indication" includes any information regarding the path/branch within the microcode trace.

Similarly, Harris discloses a priority tag that is associated with instruction path priorities (FF 10). Thus, we find that the claimed "liveness indication" reads on Harris' priority tag. As noted *supra*, Kling discloses microcode traces for storing instruction information (FF 8-9). Thus, we find that the combined teachings of Tran, Kling and Harris reasonably teach a microcode operation stored in the one or more microcode traces includes an associated liveness indication.

Therefore, Appellants have *not* persuaded us of error in the Examiner's conclusion of obviousness for representative claim 11. Therefore, we affirm the Examiner's § 103 rejection of dependent claim 11, and of claims 12, 13, 14, 26, and 38, which fall therewith.

V. CONCLUSIONS

We conclude that Appellants have *not* shown that the Examiner erred in rejecting claims 1-41.

Thus, claims 1-41 are not patentable.

VI. DECISION

In view of the foregoing discussion, we affirm all of the Examiner's rejections of claims 1-41.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv) (2007).

AFFIRMED

PEB

MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL (AMD)
P.O. BOX 398
AUSTIN TX 78767-0398